UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,872	02/12/2002	Yoshie Kanamori	100021-00069	2414

7590 05/21/2003

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER
NGUYEN, LONG T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,872	KANAMORI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-20,22-25 and 27-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,8-10,16-20,22,27-29 and 35-37* is/are allowed.

6)☒ Claim(s) *4-6,11-15,23-25,30-34,38 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 2/12/03 has been received and entered in the case.

2. Due to the newly amendment filed on 2/12/03, the drawings are objected to because the drawings does not show every feature of the invention specified in the claims.

3. Due to the newly amendment filed on 2/12/03, claims 4-6, 11-15, 23-25, 30-34 and 38-39 are rejected under 35 U.S.C. 112, 2nd paragraph, in this office action.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a fourth transistor as recited in claims 4-6 and 23-25; the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a fifth transistor as recited in claims 11 and 30; the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a sixth transistor as recited in claims 12-13 and 31-32; the differential amplifier which including a third transistor for keeping a minute

current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a seventh transistor as recited in claims 14 and 33; and the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including an eighth transistor as recited in claims 15 and 34 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 4-6, 11-15, 23-25, 30-34 and 38-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 4. Note that the independent claim 1 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit.

However, Figure 11A does not show a fourth transistor for supplying a drive current, wherein the fourth transistor is connected in parallel with the third transistor. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because no such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 4 cannot be read on any of the circuits. Thus, claim 4 is indefinite.

Claims 5 and 6 are indefinite because they include the indefiniteness of claim 4, i.e., there is no such fourth transistor.

Claim 11 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 11. Note that the independent claim 1 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a fifth transistor as recited in claim 11. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 11 cannot be read on any of the circuits. Thus, claim 11 is indefinite.

Claim 12 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 12. Note that the independent claim 1 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second

transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a sixth transistor as recited in claim 12. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 12 cannot be read on any of the circuits. Thus, claim 12 is indefinite.

Claim 13 is indefinite because it includes the indefiniteness of claim 12.

Claim 14 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 14. Note that the independent claim 1 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a seventh transistor as recited in claim 14. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 14 cannot be read on any of the circuits. Thus, claim 14 is indefinite.

Claim 15 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 15. Note that the independent claim 1 reads on Figure 11A, i.e., a third

transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show an eighth transistor as recited in claim 15. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 15 cannot be read on any of the circuits. Thus, claim 15 is indefinite.

Claim 23 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 23. Note that the differential amplifier circuit in the independent claim 17 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a fourth transistor for supplying a drive current, wherein the fourth transistor is connected in parallel with the third transistor. Furthermore, the differential amplifier in the independent claim 17 cannot be read on any of the other circuits (except Figure 11A) because no such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so the differential amplifier in claim 23 cannot be read on any of the circuits. Thus, claim 23 is indefinite.

Claims 24 and 25 are indefinite because they include the indefiniteness of claim 23, i.e., there is no such fourth transistor.

Claim 30 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 30. Note that the differential amplifier of the independent claim 17 as amended reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a fifth transistor as recited in claim 30. Furthermore, the differential amplifier of the independent claim 17 as amended cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 30 cannot be read on any of the circuits. Thus, claim 30 is indefinite.

Claim 31 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 31. Note that the differential amplifier in the independent claim 17 as amended reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a sixth transistor as recited in claim 31. Furthermore, the differential amplifier in the independent claim 31, as amended, cannot be read on any of the other circuits (except Figure 11A) because none of

the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 31 cannot be read on any of the circuits. Thus, claim 31 is indefinite.

Claim 32 is indefinite because it includes the indefiniteness of claim 31.

Claim 33 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 33. Note that the differential amplifier in the independent claim 17 as amended reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a seventh transistor as recited in claim 33. Furthermore, independent claim 17 cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 33 cannot be read on any of the circuits. Thus, claim 33 is indefinite.

Claim 34 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 34. Note that the differential amplifier in the independent claim 17 as amended reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show an

eighth transistor as recited in claim 34. Furthermore, the differential amplifier in the independent claim 17 as amended cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 34 cannot be read on any of the circuits. Thus, claim 15 is indefinite.

With respect to newly added claim 38, the recitation "said second power line" on line 11 lacks antecedent basis, and it is not clear whether applicant means "said first power line" or another power line different from the first power line.

With respect to newly added claim 39, the recitation "said second power line" on line 14 lacks antecedent basis, and it is not clear whether applicant means "said first power line" or another power line different from the first power line.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 38 is rejected under 35 U.S.C. 102(b) as being anticipated by Branson et al. (USP 5,508,644).

Insofar as understood in claim 38, Figure 1 of the Branson et al. reference discloses a differential sense amplifier circuit (10), which includes: a latch unit (12, 14, 16, 18) and a differential input portion (22, 20, 26, 24), wherein the differential input portion (22, 20, 26, 24)

includes a first transistor (22) and a second transistor (20) each having a first electrode (the electrode connected to transistor 26 for both transistors), a second electrode (the electrode connected to transistor 18 for the first transistor 22, and the electrode connected to transistor 16 for the second transistor 20) and a control electrode (gate); the control electrodes of the first and second transistors are supplied with a differential input signal (BL, BL/); a third transistor (26) receiving a control signal (transistor receiving a logic high Vdd at the gate) for keeping a minute current (small current that transistor 26 sinks) to flow through the first (22) and second (20) transistors is inserted between a first power line (Vss) and a common node (the node connected transistors 22 and 20 together) to which the first electrodes of the first and second transistors are connected; and an eighth transistor (24) is inserted between the first power line (Vss) and the common node to which the first electrodes of the first and second transistors are connected, the control electrode of the eighth transistor being supplied with a fourth control signal (LE)

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art (Figure 7) in view of Branson et al. (UPS 5,508,644).

Figure 7 of the applicant's admitted prior art shows a differential sense amplifier circuit which includes: a latch unit (111, 112, 121, 122) and a differential input portion (101, 122, 130) except for a minute current is kept to flow through the differential input portion. However,

Figure 1 of the Branson et al. reference discloses a differential sense amplifier circuit (10) which includes a small transistor (26) that is always on during operation of the differential sense amplifier circuit (because the gate of n-channel transistor always receive a logic high Vdd signal) to thereby sinks a small current from transistors 20 and 22 for the purpose of sensing a small voltage differential across the input terminals and suitable for use in high speed applications (see line 62 of Col.1 to line 10 of Col. 2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the differential amplifier in Figure 7 of the applicant's admitted prior art with the small transistor, as taught in Figure 1 of the Branson et al. reference, for the purpose of sensing a small voltage differential across the input terminals of the differential amplifiers and suitable for use in high speed applications.

Thus, insofar as understood in claim 38, the above combination meets all the limitations of this claim. In particularly, the combination of Figure7 of applicant's admitted prior art and the Branson et al. reference discloses a differential amplifier circuit which including the differential input portion (101-102, Figure 7 of applicant's admitted prior art) and a latch unit (112, 112, 121, 122, Figure 7 of applicant's admitted prior art), wherein: the differential input portion (101, 102) including a first transistor (101) and a second transistor (102) each having a first electrode (the electrode connected to transistor 130), a second electrode (the electrode connected to transistors 112 or 122) and a control electrode (gate); the control electrodes of the first and second transistors are supplied with a differential input signal (d, dx); a third transistor (26 as taught in Figure 1 of Branson et al.) receiving a control signal (logic high power supply Vdd signal) for keeping the minute current to flow through the first (101) and second (102) transistors is inserted between a first power line (AVS) and a common node (the node connected transistors 101 and

102 together) to which the first electrodes of the first and second transistors are connected; and an eighth transistor (170, Figure 7 of the applicant's admitted prior art) connected between a second power supply (AVD) and the common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first (101) and second (102) transistors are connected, a control electrode (gate) of the eighth transistor (170) being supplied with a fourth control signal (CK).

11. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (each of Figures 1-7) in view of Branson et al. (UPS 5,508,644) and Oklobdzija et al. (USP 6,232,810).

Insofar as understood in claim 39, the above combination (Figure 7 of applicant's admitted prior art and the Branson et al. reference as discussed in section 10 above with regard to claim 38) discloses a semiconductor device having a differential amplifier circuit, and a clock source (inherently, e.g., whichever source that is used to generate the clock signal CK in Figure 7 of the applicant's admitted prior art) generating a clock (CK) and supplying the generated clock (CK) to the differential amplifier circuit, wherein the differential amplifier circuit includes a latch unit and a differential input portion, wherein: the differential input portion (101, 102) including a first transistor (101) and a second transistor (102) each having a first electrode (the electrode connected to transistor 130), a second electrode (the electrode connected to transistors 112 or 122) and a control electrode (gate); the control electrodes of the first and second transistors are supplied with a differential input signal (d, dx); a third transistor (26 as taught in Figure 1 of Branson et al.) receiving a control signal (logic high power supply Vdd signal) for keeping the minute current to flow through the first (101) and second (102) transistors is inserted

between a first power line (AVS) and a common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first and second transistors are connected; and an eighth transistor (170, Figure 7 of the applicant's admitted prior art) connected between a second power supply (AVD) and the common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first (101) and second (102) transistors are connected, a control electrode (gate) of the eighth transistor (170) being supplied with a fourth control signal (CK). While the above combination (as discussed in section 10 with regard to claim 38) fails to disclose the semiconductor device includes a latch circuit latching an output signal of the differential amplifier circuit, the Oklobdzija et al. reference discloses that an SR latch circuit connected to the output of the differential sense amplifier to latch the output of the differential sense amplifier for the well-known purpose of making a D flip-flop circuit (see Figures 1 and 3, lines 13-15 of Col. 1, and lines 11-12 of Oklobdzija et al.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the differential sense amplifier in the above combination (Figure 7 of the applicant's admitted prior art and the Branson et al. reference) with an SR latch circuit connected at the output of the differential sense amplifier for the purpose of making a D flip-flop circuit for use in digital systems, such as processors, digital signal processors and memories. Thus, the limitation of claim 39 is met.

Allowable Subject Matter

12. Claims 1, 3, 8-10, 16-20, 22, 27-29, and 35-37 are allowed.

Claims 1 and 17 has been amended to include all the limitation of allowable claim (original claims 7 and 26, respectively) so claims 1 and 17 are allowed for the same reason as

indicated for claims 7 and 26, respectively, in the last office action, i.e., the prior art of record fails to disclose or suggest that the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by the differential amplifier circuit (see Figures 11A-11B).

Claims 3, 8-10, and 16 are allowed because they depend on claim 1.

Claims 18-20, 22, 27-29 and 35 are allowed because they depend on claim 17.

Newly added claim 36 corresponding to original claim 19 which was indicated to be allowed in the last office action. Hence, claim 36 is allowed for the same reason as indicated for original claim 19, i.e., the prior art of record fails to disclose or suggest an equalizer circuit having an input connected to the differential signal and an output connected to the differential amplifier circuit (see Figure 19).

Claim 37 is allowed because it depends on claim 36.

Response to Arguments

13. Applicant's arguments filed on 2/12/03 have been fully considered but they are not persuasive.

With respect to claims 38 and 39, applicant argues that both claims 38 and 39 require that the gate of the third transistor receives a control signal, and that the gate of transistor 26 in Figure 1 of the Branson et al. reference does not receive a control signal. However, the third transistor 26 in Figure 1 of the Branson et al. reference meets all the functional limitation "for keeping a minute current to flow through the first and second transistors of the differential input portion", so for broad reasonable interpretation, the gate of transistor 26 in Figure 1 of the

Branson et al. reference receives a control signal (i.e., a signal which is always high since it always connected to Vdd).

Conclusion

14. Because claims 4-6, 11-15, 23-25 and 30-34 are misdescriptive as discussed above with respect to the rejection under 35 U.S.C. 112, 2nd paragraph, these claims cannot be indicated allowable.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action (i.e., due to the amendment which causes claims 4-6, 11-15, 23-25 and 30-34 to be indefinite and also causing the drawings to be objected to, and newly added 38-39). Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

May 16, 2003

LN

Long Nguyen
Art Unit: 2816

Terry D. Cunningham
Primary Examiner